

- Sketch the Finite State Machine diagram (in ASM form) given the sequential algorithm (for $n = 8$). (18 pts.)
 - ✓ The process begins when s is asserted, at this moment we capture DA and DB on register a_i and b_i (respectively). Then the process continues by updating a_i and b_i and it is concluded when $a_i = b_i$. The signal done is asserted when the result is computed and appears on output GCD .

- Complete the timing diagram where $n = 8$. DA and DB are provided as unsigned decimals. You can provide a_i and b_i as unsigned decimals. (12 pts.)

